REMARKS

Claims 1-8 are pending. By this Amendment, claim 1 is amended, and dependent claims 7 and 8 are added. Claim 7 depends from claim 1, and claim 8 depends from claim 4.

The July 30, 2003 Office Action rejects claims 1-6 under 35 U.S.C. §103(a) as being unpatentable over Hawkins et al. in combination with the Applicant's Admitted Prior Art (AAPA). Two patents to Hawkins et al. are of record, and regrettably, the Office Action does not indicate upon which patent the rejection is based.

In an attempt to clarify the record, the October 7, 2003 Communication indicates that the rejection is based on Hawkins et al. 5,563,801. U.S. Patent No. 5,563,801 was granted to Lee et al., not Hawkins et al. Lee et al. is not of record.

In order to advance the application, the Applicant will assume that the Patent Office intended to apply U.S. Patent No. 5,556,801 granted to Hawkins et al. since:

1. It is one of the two patents to Hawkins et al. that are of record;

2. Patent No. 5,563,801 to Lee et al. has a patent number that is closer to U.S. Patent No. 5,556,801 (to Hawkins et al.) than the other Hawkins et al. patent of record.

3. U.S. Patent No. 5,556,801 depicts reference numerals that correspond to the reference numerals cited in the July 31, 2002 Office Action.

Accordingly, it will be assumed that the Office Action refers to U.S. Patent No. 5,556,801 (hereinafter, Hawkins et al.). The Patent Office is respectfully requested to clarify in the next responsive communication that the July 30, 2003 Office Action refers to U.S. Patent No. 5,556,801 to Hawkins et al.

This rejection is respectfully traversed.

1. Neither Hawkins et al. in view of the Applicant's Admitted Prior Art (AAPA) nor the AAPA in view of Hawkins et al. discloses, teaches or suggests "a method of manufacturing a charge-coupled image sensor" that includes forming:

> in a silicon slice ... channel-shaped semiconductor regions running in a first direction

and forming

> a system of strip-shaped electrodes is formed on the gate dielectric, said strip-shaped electrodes running in a second direction which is substantially perpendicular to the first direction,"

wherein the method is

> characterized in that the channel-shaped semiconductor regions are not formed in the silicon slice until after the gate dielectric has been provided on the surface of the silicon slice, the ions of the dopants being implanted through the gate dielectric and the channel-shaped semiconductor regions are formed in the silicon slice before the strip-shaped electrodes are formed on the gate dielectric

as specified in claim 1 and therefore contained in claims 2 and 3 dependent on claim 1.

2. Neither Hawkins et al. in view of the Applicant's Admitted Prior Art (AAPA) nor the AAPA in view of Hawkins et al. discloses, teaches or suggests "a method of manufacturing a charge-coupled image sensor" that includes forming:

> forming a plurality of elongate channels in the silicon slice by implanting dopant ions through the gate dielectric into the silicon slice, the channels being formed so as to adjoin the surface; and
>
> forming a system of elongate gate electrodes on the gate dielectric after the channels are formed, the elongate electrodes being formed transversely to the channels

as specified in claim 4, and therefore contained in claims 5 and 6 dependent on claim 4.

3. The only semiconductor regions of Hawkins et al. that are formed in the silicon slice by implant through a pre-existing gate dielectric are regions 32. Regions 32 are not channel-shaped semiconductor regions. The only strip-shaped electrodes of Hawkins et al. that are formed after formation of regions 32 are electrodes 40a shown in FIG. 2F of Hawkins et al.

Electrodes 30a are formed prior to implant at the step depicted in FIG. 2C, and electrodes 30a function as a mask for a later implant.

In Hawkins, et al., strip-shaped electrodes 40a cannot run in a second direction which is substantially perpendicular to the direction of regions 32, as required by claim 1, since both the regions 32 and the electrodes 40a are defined by the edges of electrodes 30a. Regions 32 are formed by implanting between electrodes 30a which serve as a mask. Regions 32 cannot therefore be regarded as the claimed channel-shaped semiconductor regions.

Should regions 32 be read as channel-shaped semiconductor regions, they must be regarded as running parallel to electrodes 30a. Then, gate electrodes 40a would have to be formed by first depositing poly over and in the trench between electrodes 30a and then chemical mechanical polishing (CMP) the surface to leave only electrodes 40a in the trench between electrodes 30a. Then, if electrodes 40a were to be read as the claimed strip-shaped gate electrodes, then electrodes 40a also must be regarded as running parallel to electrodes 30a. Regions 32 and electrodes 40a are self-aligned with the edges of electrodes 30a which defines the directions of both the regions 32 and the gate electrodes 40a to be parallel, not substantially perpendicular, to each other. In fact, this self-alignment feature is the intended purpose of the Hawkins et al. disclosure.

The scope and content of Hawkins et al. does not disclose "channel-shaped semiconductor regions running in a first direction" and "strip-shaped electrodes running in a second direction which is substantially perpendicular to the first direction."

4. Then, the Office Action asserts that the "Applicant admits the process of forming strip-shaped semiconductor regions, in a first direction by implantation through an oxide layer followed by removal of the oxide layer and formation of a gate dielectric upon which is formed strip-shaped gate electrodes running perpendicular to the first direction to have been known prior to applicant's invention." This assertion is not exactly accurate.

The specification states "After the formation of these semiconductor regions [including strip-shaped channels], the surface of the slice is provided with a gate dielectric comprising a

layer of a thermally formed silicon oxide and a silicon nitride layer deposited thereon. A system of polycrystalline silicon electrodes directed transversely to the channels is formed thereon." See page 1, lines 14-18. The specification further describes that "the slice is provided ... with a thin layer of silicon oxide, also referred to as a pad oxide. Subsequently, a photoresist mask is formed on the layer of pad oxide, after which the implantation of ions of a dopant is carried out, the photoresist mask is removed, a thermal treatment is carried out and, finally, the layer of pad oxide is etched away." See specification page 1, lines 20-24. The specification does not disclose that it is prior art to implant dopant ions through the pad oxide. It fact, it is inherent that during the thermal treatment, dopant ions in the pad oxide will diffuse into the silicon slice. Furthermore, the specification does not disclose that the implant is performed after the gate dielectric layer is provided.

5. The Office Action attempts to argue the Hawkins et al. teaches how to modify the AAPA to become the claimed method. However, Hawkins et al. does not teach implanting a channel through a gate dielectric layer. Instead, Hawkins et al. teaches only implanting biasing regions to assist in charge transport of a two phase CCD. The biasing implant regions 32 are disposed in pre-existing channels (existing before the gate dielectric layer is formed) and spaced between a pattern of half electrodes 30a. Then, the other half electrodes 40a are inter-digitally formed and electrically connected to the first half electrodes (see column 7, lines 43-49).

The biasing implant regions are not oriented in the direction of the channel. In fact, the biasing implant regions are oriented transverse to the channel since electrodes 30a are oriented transverse to the channel.

The Office Action appears to be arguing that it would be obvious to modify the AAPA process of implanting dopant ions in the pad oxide to become a process that implants dopant ions through a gate dielectric layer (instead of in a pad oxide) to form the strip-shaped semiconductor regions. The Office Action appears to assert that Hawkins et al. teaches a process that implants dopant ions through a gate dielectric layer (instead of in a pad oxide) to form the strip-shaped

semiconductor regions. If applicable to the channel-shaped semiconductor regions specified in present claim 1, this assertion is respectfully traversed.

Contrary to the Office Action's assertion, Hawkin et al. does not teach implantation of channels through a gate dielectric layer. In particular, Hawkins et al. teaches forming channels of a second conductivity type in a substrate of a first conductivity type (see column 4, lines 5-8), and the channels are formed before a gate dielectric layer is formed (see column 5, lines 52-59). Hawkins et al. does not disclose, teach or suggest forming channels after a gate dielectric layer is formed. In Hawkins et al. the channels are formed before the gate dielectric layer is formed. Region 32 of Hawkins et al. is merely a biasing implant within the buried channel (see column 4, lines 32-35 and column 6, lines 22-40).

The AAPA discusses three distinct implant processes performed before the gate dielectric layer is formed. First, a p-well is formed. Second, n-type channel-shaped semiconductor regions are formed in the p-well. Third, p-type channel stops are formed separating the n-type channel-shaped semiconductor regions. In the AAPA process, the n-type channel-shaped semiconductor regions are formed in the silicon slice before the channel stops are formed and before a gate dielectric layer is formed. The first two of the three implant steps described by the AAPA are the same steps as described in Hawkins et al. The third step, forming a channel stop, is not discussed by Hawkins et al.

6. Even if, *arguendo*, Hawkins et al. were to be regarded as teaching implantation of channels (in contrast to biasing region 32) through a gate dielectric layer, the AAPA process modified to implant channels by the method that Hawkins et al. uses to implant biasing regions, the resulting modified process would still not achieve the claimed method.

According to the process of Hawkins et al. (i.e., implantation of biasing regions through a gate dielectric layer), thick conductive electrodes (e.g., 30a) with nearly vertical side walls are required (see column 4, lines 9-11 and column 5, line 63 through column 6, line 20). If the channels were to be formed by the implant through the gate dielectric layer according to the Hawkins et al. process of forming biasing regions, the conductive electrodes 30a of Hawkin et al.

would have to be formed on the gate dielectric layer and oriented parallel with the desired direction of the channel. In the AAPA process, gate electrodes are oriented transversely to the channel-shaped semiconductor regions. Conductive electrodes 30a cannot therefore be regarded as the gate electrodes since the gate electrodes are required to be oriented transversely to the channels of the AAPA process.

The only other electrodes described by Hawkins et al. are conductive electrodes 40a. The teaching of Hawkins et al. is that deposited conductive poly layer 40 is planarized to form electrodes 40a (see column 4, lines 18-24 and column 6, line 59 through column 7, line 40). Such planarized conductive poly layer 40 would leave conductive electrodes 40a inter-digitally formed between electrodes 30a. Here again, conductive electrodes 40a would be parallel with the channel, not substantially perpendicular as specified in claims 1 and 4.

For electrodes 40a to be regarded as the gate electrodes of the AAPA process, conductive electrodes 40a would have to be oriented transversely to the channel direction. Orienting conductive electrodes 40a transversely to the channel direction requires that conductive electrodes 40a overlie the conductive electrodes 30a in a crossing pattern. Then, planarization would cut electrodes 40a into small segments that fit between the electrodes 30a. They could not function as gate electrodes.

7. Furthermore, the applied art does not disclose, teach or suggest any motivation for forming channels through a gate dielectric film. In fact, Hawkins et al. teaches forming channels before the gate dielectric layer is formed. Only bias implant regions 32 are formed through the gate dielectric layer, and regions 32 do not constitute a channels.

The Office Action asserts that "disclosing formation of electrodes [as Hawkins et al. does] on a nitride oxide gate dielectric through which implantation has been performed ...[provides] motivation to implant through a retained nitride/oxide gate dielectric material as opposed to the sacrificial oxide material of the admitted prior art process." To the contrary, the Office Action fails to apply any reference that can be considered evidence of a motivation for modification as discussed above.

To establish a case of obviousness, the Patent and Trademark Office must demonstrate by substantial evidence that the prior art relied upon, coupled with the knowledge generally available in the art at the time of the invention, contains some suggestion or incentive that would have motivated an ordinarily skilled person to modify the subject matter of a reference or combine the subject matters of the references to achieve the claimed subject matter. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). M.P.E.P. 2143.01 instructs that "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." "[T]he central question is whether there is reason to combine references," *McGinley v. Franklin Sports, Inc.*, 262 1339, 1351-52, 60 1001, 1008 (Fed. Cir. 2001). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)." See M.P.E.P., section 2143.01, page 2100-98, Rev. 1, Feb. 2000, 7th Ed (emphasis in the original).

"[A] showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding'," *Brown and Williamson Tobacco Corp. v. Phillip Morris Inc.*, 229 F.3d 1120, 1124-1125, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000). "[T]here must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant," *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed Cir. 1998). "[T]eachings of references can be combined only if there is some suggestion or incentive to do so," (emphasis in original), *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Motivation must be found with specificity. "[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention would have selected these components for combination in the manner claimed," *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). "[E]ven when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the

claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious," *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998). The Patent Office can satisfy this burden of showing the obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references," *In re Fitch*, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992).

Establishment of a suggestion or incentive to modify or combine prior art references requires substantial evidence of such suggestion or incentive. "The factual question of motivation is material to patentability, and could not be resolved on subjective belief of unknown authority," *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002). Office Action assertions of such suggestion or motivation, without evidentiary support, is merely subjective belief and is insufficient to constitute substantial evidence upon which a legal conclusion can be based.

In re Lee describes a two fold requirement for the Board of Patent Appeals and Interferences to establish a motivation to modify. First, the Board must make reasoned findings of fact, based on evidence on record. Second, the Board must also explain the reasoning by which the findings are deemed to support the Board's conclusion. It should be noted that these are requirements imposed on decisions of the Board, not decisions of the examiner corps. However, the examiner corps must still make the record (e.g., applied art teaches ...) upon which the factual findings of motivation can be based.

8. With regard to claims 2 and 5, Hawkins et al. does not disclose the method of forming the silicon nitride part of the gate dielectric according to the present invention, namely Low Pressure Chemical Vapor Deposition as specified by claims 2 and 5, and therefore contained in claims 3 and 6 dependent thereon.

Furthermore, with regard to claims 3 and 6, Hawkins et al. does not disclose, teach or suggest any motivation to alter the thickness of the prior art silicon nitride part of the gate

dielectric. In fact, Hawkins et al., at one location (see column 9, lines 14-15), discloses that said silicon nitride is between 5 and 30 nm. Hawkins et al. does not disclose, teach or suggest that the claimed method forms the silicon nitride part of the gate dielectric to a thickness of at least 50 nm as specified by claims 3 and 6.

The July 30, 2003 Office Action does not assert any basis for its rejection of claims 2-3 and 5-6. Accordingly, withdrawal of the rejections of claims 2-3 and 5-6 is earnestly solicited.

CONCLUSION

In view of the present amendments and remarks, withdrawal of the rejection of the claims is earnestly solicited. It is respectfully submitted that the present application is in condition for allowance. Prompt reconsideration and allowance of the application are earnestly solicited. Should the examiner believe that any further action is necessary to place the application in condition for allowance, the examiner is invited to contact the undersigned applicant representative at the telephone number listed below.

The Commissioner is hereby authorized to charge any fees (or credit any overpayment) associated with this communication to Deposit Account No. 04-1425.

Respectfully submitted,

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